

METHOD AND SYSTEM FOR PHASE OFFSET CANCELLATION IN MULTI-PHASE CLOCK GENERATOR CIRCUITS

FIELD OF THE INVENTION

The present invention relates generally to integrated circuits and more particularly to phase offset cancellation techniques for use with multi-phase clocks.

5 BACKGROUND OF THE INVENTION

Multi-phase clock generators have a wide range of applications in radio-frequency (RF) and mixed-mode (MM) circuits. For example, many RF communications circuits use quadrature amplitude modulation (QAM) for efficient use of the channel bandwidth. A QAM modulator uses an inphase and quadrature phase component of a RF frequency, which
10 are 90 degrees apart in phase, to modulate two stream of base-band data with bandwidth of Δf in a single channel of Δf .

In serial wireline communication circuits, lower frequency multi-phase clocks can be used to serialize or deserialize the low-speed parallel data into a high-speed serial stream of data. Figure 1 is a diagram that illustrates a multi-phase sampling scheme for serial link
15 communications. As is seen, there is an input data line 12 which is coupled to a plurality of component clock signals ck0-ck4. Each clock 14a-14d is coupled to a respective sampler (16a-16d). Each clock 14a-14d clocks the sampling instant that its respective sampler will use to determine the value of the input data line 12. As is also seen, there are wave forms that represent a set of component clock signals 18a-18d for the multi-phase clock that
20 correspond to clock signals 14a-14d respectively. As is seen, each sampler samples the data from data line 12 on the rising edge. The advantage of using multi-phase clock generators in

multi-gigabit serial links is generating an on-chip multi-GHz clock.

However, a major problem that can limit the use of multi-phase clock generation for high-speed data communication or RF communication is the phase offset between the adjacent clock phases, which directly degrades the performance of the system.

5 Figure 2 is a block diagram illustrating the same sampling scheme as Figure 1, except there are phase offsets, for example, as shown, samplers 14a', 14b' and 14c'. As is seen, in this diagram only sampler 14d receives the full data signal. This phase offset is caused by a number of sources, including but not limited to, mismatch in different stages of a multi-stage oscillator, the oscillator clock buffers, and periodic ripples on the oscillator or
10 buffers control signal and supply voltage.

In QAM systems, phase offset between inphase and quadrature phases results in interference between the two quadrature RF bands of data. In serial communication, phase offset shows up as a timing error that degrades system performance both in the transmitting and receiving of data. In data transmission using multiple phases, phase error among clock
15 phases causes a data symbols to be longer and a symbol to be shorter than the idea symbol width. The shorter data symbols are harder to be detected by the receiver as they have less timing margin. In the receiver, multiple clock phase error results in timing error in sampling of data that effectively increases system bit error rate (BER) by sampling the data symbol at a non-ideal point.

20 Other techniques have been adopted in the past to address the phase offset problem in multi-phase clock generators. For example, a technique proposed in C.-H. Park, et. al., "A 1.8GHz Self-Calibrated Phase-Locked Loop with Precise I/Q Matching," IEEE JSSC, May 2001, pp. 777-783, has the advantage that it used only one phase detector to correct all

phases, by switching the phase detector to measure the difference between a reference signal and multiple phases from a multi-stage oscillator at a time, and apply the output of the phase detector to the corresponding delay adjusting circuit for that phase. The advantage of this scheme is that it does not suffer from mismatches in the phases detector. However, a major drawback of this approach is that the phases from the multi-stage oscillator go through multiple stages of retiming and multiplexing before final correction by the phase detector loop.

As a result, although the phase offset of the clock phases after the retiming and multiplexing stages are zero, the original phase will still experience some phase error due to mismatch in different retiming and multiplexing paths for each phase. In addition, this scheme is much more complex in implementation and the active area used in the scheme is more than an order of magnitude larger than the proposed design in this application.

Another approach as proposed in L. Yu and W. M. Snelgrove entitled "A novel adaptive mismatch cancellation system for quadrature IF radio receivers," IEEE Trans. Circuits Syst. II, June 1999, pp. 789-801, adds complexity in the clock signal path that limits the performance of the system, is also limited to just few applications, e.g. image rejection in RF systems.

Finally, an approach proposed in B. Razavi, "Design considerations for direct-conversion receivers," IEEE Trans. Circuits Syst. II, June 1997, pp. 428-435, has the advantage of simplicity of design and does not introduce complexity in the clock signal path, however, it does not offer a continuous adjustment during circuit operation. This is a serious drawback for circuits that are sensitive to temperature and voltage variations during operation.

Accordingly, what is needed is a system and method for minimizing phase offset in a communications circuit that overcomes the above-identified problems. The system should be competitive with existing integrated circuits, should be easily implemented and cost effective. The present invention addresses such a need.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a diagram that illustrates a multi-phase sampling scheme for serial link communications.

10 Figure 2 is a block diagram illustrating the same sampling scheme as Figure 1, except there are phase offsets.

Figure 3 illustrates a first embodiment of a phase-offset cancellation mechanism in accordance with the present invention.

Figure 4 illustrates a second embodiment of a phase offset cancellation mechanism.

15 Figure 5 is a diagram for a subtractor and two phase detectors in accordance with the present invention.

Figure 6 is a mechanism for device mismatch cancellation in accordance with the present invention.

DETAILED DESCRIPTION

20 The present invention relates generally to integrated circuits and more particularly to phase offset cancellation techniques for use with multi-phase clocks. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various

modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the principles and features described herein.

5 A system for use with a multi-phase clock generator is disclosed. It should also be understood that the multiphase clock generator can be a phase lock loop (PLL), delay lock loop (DLL), or any other circuit capable of providing a multiphase clock. The system comprises at least two phase detectors coupled to the multi-phase clock generator for receiving component clock signals of the multi-phase clock generator, wherein at least some of the component clock
10 signals are offset from each other in phase. Each of the phase detectors detects phase differences between pairs of component clock signals. The system includes a summer coupled to the at least two phase detectors for measuring the phase differences between the at least two phase detectors. The system includes at least one variable delay element for receiving the measured phase difference and for providing a delay which is proportional to an output value
15 of the summer. The delay is used to reduce the phase differences.

 In a preferred embodiment of a system and method in accordance with the present invention, adjacent phase differences are equalized utilizing a phase cancellation mechanism for multi-phase clock generator circuits. In this circuit each phase detector within the phase cancellation mechanism measures the phase spacing of the two component clock signals,
20 and the difference between the two component clock signals is applied to an adjustable delay element by a subtractor to cancel the phase error of a particular stage. In so doing, phase offsets can be cancelled in multi-phase clock generator in an efficient and effective manner.

 In a preferred embodiment of a system and method in accordance with the present

invention, adjacent phase differences are reduced utilizing a phase cancellation mechanism.

Therefore, the phase of a component clock signal, cki0, is fixed as the phase reference, and the phase of a next component clock signal, cki1, is adjusted in such a way that the phase difference between a first adjacent pair of clocks is equal to a next adjacent pair of clocks.

5 The same mechanism may be used to adjust a next component clock signal ck2, and so on.

Each phase detector within the phase cancellation mechanism measures the phase spacing of the two adjacent clocks, and the difference between the two adjacent phase spacings is applied to an adjustable delay element by a subtractor to cancel the phase error of a particular component clock signal.

10 To describe the features of the present invention in more detail, refer now to the following description in conjunction with the accompanying figures. Figure 3 illustrates a first embodiment of a phase-offset cancellation mechanism 100 in accordance with the present invention. Figure 4 illustrates a second embodiment of a phase cancellation circuit 200 in accordance with the present invention. As is seen, since the output of each of the
15 phase detectors 204a –204d is a current instead of a voltage a separate phase detector per input of the summing block is required. Either of the phase-offset cancellation mechanisms 100 or 200 can be coupled to the multi-phase clock generator 10 of Figure1 via the serial line input data line 12 to provide the appropriate phase-offset cancellation.

Each of these embodiments illustrate a four-phase system with almost equal phase
20 spacings provides the offset cancellation scheme. The four component clock signals (cki0 to cki3) can be the output of a multi-phase clock generation circuit that experience phase errors due to the mismatches in the clock generation circuit and its following buffers. It should be understood that, although the present invention is described with respect to a four-phase

system, the same architecture can be extended to any equally spaced multiple phase system and it would be within the spirit and scope of the present invention.

Referring back to Figure 3, there are a plurality of adjustable delays 102a-102d, a plurality of summers, 106a-106c, and a plurality of phase detectors 104a-104d. In this embodiment, component clock signal cki0 is input to adjustable delay 102a, and it provides an output of component clock signal ck0. That output is provided to phase detector 104a. As is also seen, a cki1 is provided to an adjustable delay 104a and it provides an output component clock signal ck1. The output from phase detector 104a (pd0) is provided to summer 106a.

A negative output from summer 106a is provided to a positive input of summer 106b. The output from summer 106a (pd01) is provided to the adjustable delay 102b. The output (pd1) of the phase detector 104b is also provided to the positive input summer 106b. The output (pd1) of summer 106b is provided to adjustable delay 102c. The input of adjustable delay 102c is component clock signal cki2. The output of adjustable delay 102c is provided to the phase detector 104b and phase detector 104c. The phase detector 104c provides an output (pd2) to the negative input of summer 106c. The negative output of summer 106b is provided to the positive input of summer 106c. The input to adjustable delay 102d is component clock signal cki3. The output (pd23) from summer 106 is provided to adjustable delay 102d. The output from adjustable delay 102d is provided to the input of phase detector 104c and the input of phase detector 104d. The output from adjustable delay 102a is also provided to the phase detector 104d.

The phase detectors 104a-104d convert the phase difference between two component clock signals into a proportional current, and the analog subtractor within the summers 106a-106c uses the current difference from two adjacent phase detectors to charge and discharge a

capacitor (not shown) at its output.

Accordingly, a key feature of a preferred embodiment of the present invention is to equalize every two adjacent phase differences. Therefore, the phase of the first component clock signal, $cki0$, is fixed as the phase reference, and the phase of the next component clock signal, $cki1$, is adjusted in such a way that the phase difference between component clock signal $ck0$ and component clock signal $ck1$ ($pd0$) is equal to component clock signal $ck1$ and component clock signal $ck2$ ($pd1$). The same mechanism may be used to adjust the next clock phase $ck2$, and so on. Each phase detector 104a-104d measures the phase spacing of the two adjacent clocks, pdi , and the difference between pdi and $pdi+1$ is applied to the adjustable delay element by a subtractor to cancel the phase error of that stage. It should be noted that in alternative embodiments of the present invention, the techniques described herein may be used to equalize phase differences between any one or more pairs of component clock signals.

To describe the features of the phase detector and subtractor in more detail refer now to the following description in conjunction with the accompanying figures. Figure 5 is a diagram for a subtractor and two phase detectors 306a and 306b in accordance with the present invention. Each phase detector 306a and 306b generates a current pulse whose width is proportional to the phase difference between the two input component clock signals, as the current only flows into the branch when both switches 312a, 312b and 314a and 314b atop the current source 308a and 308b are closed at the same time. The subtraction is performed using current summing of the current from the right branch and inverted current from the left branch through a mirror circuit 310. If one phase difference is larger than the other phase difference, voltage on the capacitor 322 will change in a direction to move the common

clock edge, e.g., component clock signals $ck1$, in the two pairs of clock phases, e.g. $ck0/ck1$ and $ck1/ck2$, to correct for this difference through the adjustable delay element.

Any additional phase offset is a result of the mismatches in the phase detector 306a, 306b and subtractor combination. The main source of mismatch in this circuit is mismatch
5 between the two current sources 308a and 308b and the mirror circuit 310. Since these elements are not needed to operate at a very high frequency, they can be implemented with very large device sizes to maximize the matching.

To further reduce the effect of mismatch in the phase detector current sources and mirror devices, a device mismatch cancellation scheme is implemented to cancel out the
10 offset in the current pulses at the output of the circuit. Figure 6 is a mechanism for device mismatch cancellation in accordance with the present invention. In this scheme, as shown in Figure 4, the current sources 308a' and 308b' in the phase detectors 306a' and 306b' are adjustable DACs (digital to analog converters), whose amplitude can be digitally adjusted to compensate for the mismatch in the down (I_{pd1}) and up (I_{pd0}) current at the output nodes
15 when the input clocks have the same phase difference.

During the calibration mode when the calibration signal is high, the inputs to the two phase detectors 306a' and 306b' are exactly the same (i.e. both sides receive $ck0$ and $ck1$) with devices 402a, 402b and 404a, 404b respectively. Therefore, in an ideal circuit without any device mismatch, the up and down current pulses dump the same amount of charge into
20 the capacitor in opposite directions that cancel out each other and capacitor voltage does not change. In the instance of a mismatch, the current in one branch is higher than the other and thus the net charge dumped into the capacitor (not shown) decreases or increases continuously till it reaches ground (0V) or supply voltage (V_{dd}). A controller (not shown)

senses the output of the circuit (V_{pd10}) and searches for an adjustment setting in the digitally controlled current sources to find the setting where V_{pd10} moves from one supply rail to another (e.g. V_{dd} to ground). That setting is the one that minimizes the circuit offset due to mismatch.

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Conclusion

In a system and method in accordance with the present invention, adjacent phase differences are equalized utilizing a phase cancellation mechanism for multi-phase clock generator circuits. In this circuit each phase detector within the phase cancellation
10 mechanism measures the phase spacing of the two component clock signals, and the difference between the two component clock signals is applied to an adjustable delay element by a subtractor to cancel the phase error of a particular stage. In so doing, phase offsets can be cancelled in multi-phase clock generator in an efficient and effective manner.

Accordingly, the multi-phase clock generator after the phase offset has been
15 cancelled can be utilized in a variety of applications including but not limited to (1) a transmit clock used for timing a driver in a transmitter; (2) a receiver clock used for timing a sampler in a receiver; (3) in a transceiver circuit where one or both of the transmit and receive portions are timed by the multi-phase clock; or (4) in a communication channel having a transmitter and a receiver, where one or both of the transmitter and receiver use a
20 multi-phase clock that has been phase cancelled.

Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the

present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.